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New features of the PSI46

1. Features

The new version of the Pixel readout chip (PSI46) has several new features. It is built using 0.25µ IBM process. The new chip has 38 pads. Three smaller pads (65 x 90µ) are intended for the fallback option of using separate clock signal for serial control interface. PSI claims that the interface works with 40 MHz common timing clock input. We will be able to use both options during debugging and decide later which one to use during wafer test. The remaining 35 bigger pads (120 x 168µ) are wire bond pads. Table 1 lists PSI46 pads below. The PSI46 has different number of pixel rows due to increase in the number of pixels. There are 80 rows now instead of 53 as compared to the PSI43.

Table 1 PSI46 pad assignment

	Pad No.	Signal name	Signal level	Comment
1	a	i2c_clk+	diff. Vcm = 1V	Vd = 600 mV
2	b	i2c_clk-	diff. Vcm = 1V	Vd = 600 mV
3	c	i2c_clk_sel	CMOS	0 to Vd
4	1	GND_CAP	N/A	ground pad for cap
5	2	GND	N/A	
6	3	token_in+	diff. Vcm = 1V	Vd = 600 mV
7	4	token_in-	diff. Vcm = 1V	Vd = 600 mV
8	5	reset	CMOS	0 to Vd
9	6	aout+	differential analog	500 ohms load
10	7	aout-	differential analog	500 ohms load
11	8	GND	N/A	
12	9	trig_out+	differential analog	500 ohms load
13	10	trig_out-	differential analog	500 ohms load
14	11	CAP_VD+	N/A	bypass cap
15	12	cal_trig_res+	diff. Vcm = 1V	Vd = 600 mV
16	13	cal_trig_res-	diff. Vcm = 1V	Vd = 600 mV
17	14	clk+	diff. Vcm = 1V	Vd = 600 mV
18	15	clk-	diff. Vcm = 1V	Vd = 600 mV
19	16	VA+	N/A	1.8V nominal
20	17	VA+	N/A	1.8V nominal
21	18	VC+	N/A	Connect to VD+
22	19	GND	N/A	
23	20	GND	N/A	
24	21	CAP_DAC	N/A	bypass cap
25	22	i2c_a3	CMOS	0 to Vd
26	23	i2c_a2	CMOS	0 to Vd
27	24	i2c_a1	CMOS	0 to Vd

28	25	i2c_a0	CMOS	0 to Vd
29	26	i2c_dat+	diff. Vcm = 1V	Vd = 600 mV
30	27	i2c_dat-	diff. Vcm = 1V	Vd = 600 mV
31	28	token_out+	diff. Vcm = 1V	Vd = 600 mV
32	29	token_out-	diff. Vcm = 1V	Vd = 600 mV
33	30	CAP_dig_reg	N/A	bypass cap
34	31	VD+	N/A	2.5V nominal
35	32	VD+	N/A	2.5V nominal
36	33	GND	N/A	
37	34	GND	N/A	
38	35	GND_CAP	N/A	ground pad for cap

2. Registers

Most of the registers have the same function as for PSI43. There are two completely new registers implemented in this design for detector leakage settings and temperature readings. Some registers have different meaning. See Table 2 below.

Table 2 PSI46 registers

	Name	Function	Width	Addr.	Default
		Power Supply Regulators			(hex)
1	Vdig	Digital logic power regulator	4	0x01	0F
2	Vana	Analog power regulator	8	0x02	B4
3	Vsh	Sample & Hold power regulator	8	0x03	FF
4	Vcomp	Comparator power regulator	4	0x04	0F
		Analog PUC			
5	Vleak_comp	Detector leakage current comp.	8	0x05	0
6	Vrgpr	Preamplifier feedback	4	0x06	0
7	Vwlpr	Preamplifier fb-well voltage	8	0x07	23
8	Vrgsh	Shaper feedback	4	0x08	0
9	Vwlsh	Shaper fb-well voltage	8	0x09	23
10	Vhlddel	S&H delay	8	0x0A	76
11	Vtrim	Pixel trim range	8	0x0B	1D
12	Vthrcomp	Pixel comparator threshold	8	0x0C	5A
		Pixel Readout			
13	Vbias_bus	DC-readout bias current	8	0x0D	26
14	Vbias_sf	Pixel to DB sf-current	4	0x0E	6
		Double Column Readout			
15	Voffsetop	Offset voltage	8	0x0F	4B
16	Vibiasop	On current	8	0x10	6E
17	Voffsetro	Offset voltage	8	0x11	4B
18	Vion	On current	8	0x12	72
		Chip Readout			
19	Vbias_ph	Pulse height differential ampl.	8	0x13	66
20	Ibias_dac	DAC event multiplexer	8	0x14	BC

21	Vlbias_roc	Chip readout amplifier	8	0x15	C8
		Fast Trigger			
22	Vlocolor		8	0x16	64
23	Vnpix		8	0x17	64
24	Vsumcol		8	0x18	64
		Miscellaneous			
25	Vcal	Test pulse amplitude	8	0x19	14
26	CalDel	Test pulse delay	8	0x1A	64
		Write-Only Digital Registers			
27	RangeTemp		8	0x1B	0
28	WBC	Trigger latency	8	0xFE	1B
29	CTRL_REG	Control register	8	0xFD	0

3. Default settings

Table 2 provides recommended initial settings for PSI46. Note that the settings for internal voltage regulators cannot be varied to change chip's behavior because of the bug in the design. The power supplies have to be set as shown in the Table 3. Adjust them if necessary to stabilize the chip's internal voltage regulators.

Table 3 Power supply settings

Power supply	Output Voltage [mV]	Nominal Current [mA]	Comment
VA	1500	24	regulators saturated
VD	2000	28..30	regulators saturated

4. Serial Command Interface

There are no changes in command structure for PSI46. There are still four (4) commands used to setup the chip. These are Prog_DAC, ClrCal, Prog_Pix and Cal_Pix. The Prog_DAC and ClrCal are identical to the PSI43 commands. The Cal_pix and Prog_Pix are quite different. A binary value of the column address (ColAdr) is encoded in the following manner: <ColAdr> = grey (double column) + 0/1 for left right column. The upper five bits of the ColAdr are formed by a Grey code of the double column address and the lower bit is set to zero or one depending on the column position within double column. The row address is simply greycoded as in PSI43.

5. Readout

Since this version of the chip does not provide the charge information because of another bug in the design, the only way to determine if the pixel works is by observing the hit address. Hopefully, the next version of the chip will work properly therefore, the charge measurements have to be in place anyway. The analog hit addresses are also encoded (see attachment). According to the preliminary results, the address separation and their uniformity is much better now, so this will certainly simplify decoding of hit addresses.